#10/Reconsideration ... 2/1/02

Attorney's Docket No. S1022/8250 (RAS/JHM)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Gajinder Singh PANESAR
Serial No.: 09/340,776
Filing Date: June 28, 1999
For: DESIGN OF AN APPLICATION SPECIFIC PROCESSOR (ASP)

Examiner: T. Phan
Art Unit: 2123

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Lori A. Bianczzo

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Dear Sir:

RESPONSE

In response to the Office Action mailed October 2, 2001, Applicant respectfully requests reconsideration. Claims 1-7 are currently pending in this application.

In Paragraph 1 of the Office Action, the Examiner noted that the Application Number of the certified copy of the priority document is different than that referenced in the Declaration. Applicant is currently investigating this matter. Corrected documents will be submitted in Applicant's next response.

The Office Action rejected claims 1-7 under 35 U.S.C. §102(a) as being anticipated by Bona (5,710,934). Applicant respectfully traverses this rejection.

Bona is directed to a method for developing a programmed ASIC (Application Specific Integrated Circuit). Bona discloses producing a test platform circuit board comprising a circuit fabricated around a DSP or microprocessor core, RAM memory, digital and analog data paths, a management and test program, control logic, and optionally, peripherals intended to be integrated in the final circuit (Col. 6, lines 38-49). Figs. 4A, 4B, and 4C illustrate the development process of the ASIC, as disclosed by Bona. As illustrated in Fig. 4A and described

from Col. 6, line 52 to Col. 7, line 3, Step H involves drawing up project specifications for the ASIC according to given constraints such as dimensions and price. Next, Step I involves specification and definition of the hardware and software of the ASIC corresponding to the project specifications. This step involves defining what functionality will be implemented in hardware and what functionality will be implemented in software, by processing and management programs. The processing program provides functionality for the ASIC, such as filtering and digital compression, while the management program provides for the management of the ASIC hardware and sequencing of the various software modules performed by the ASIC (Col. 3, lines, 45-50). Then, in Step J, a testability study of the hardware circuit and the software for managing the ASIC is performed and test patterns are generated. Next, the circuit is produced and simulated on a workstation and the software management program is produced and simulated on a workstation with the aid of the test patterns (Steps S & Q).

The simulation of the hardware circuit is performed using a model generated from a library supplied by the manufacturer of the circuit. Given that the same test patterns used to test the model are also used on the actual fabricated circuit, Bona suggests that the model is a lower-level model of the circuit at the transistor level, in a simulation language such as VHDL. However, nowhere does Bona disclose, teach, or suggest that this model is a functional model implemented in a high level language.

Next, in Step T, the production of program modules of the processing program and unit and global tests on a test platform is performed using the test patterns defined during the testability study. A validation of the hardware and software decisions is then performed which permits the integration of the application program for the ASIC with the management software. The steps in Fig. 4B are then performed to validate the application software in the trial ASIC shown in Fig. 4B. Masks are generated for the circuit and the circuit is manufactured. Then, electrical validation is performed using test patterning. Validation of the application logic of the application software is then performed using the file ASIC. Then, as illustrated in Fig. 4C, the closed ASIC (i.e., the ASIC including the application logic implementing the application software) is manufactured and electrical validation of the closed ASIC is performed. Finally, using the closed ASIC, the application software is validated using the test sequences on a test platform.

A block diagram of the test platform is shown in Fig. 5. The test platform includes an onboard read/write memory 112 to emulate RAM of the ASIC, an onboard read/write memory 111 to emulate ROM of the ASIC. The integrated circuit is connected to a test platform through buses 91 and 92 by interfaces 101-110. As disclosed at Col. 9, line 41 through 48, microcomputer 300 can also be used with the interface software to produce software tests which will be stored in the ROM memory. As disclosed in Bona, these tests are usually produced on a workstation with the aid of a VHDL model of the circuit. As described in Bona, by using the physical test board, these software tests can be performed in real time which is not possible when running the tests on the computer model of the circuit.

The method of simulating an application specific processor (ASP) recited in claim 1 is entirely different from the method disclosed by Bona for developing an ASIC. First, Bona contains no disclosure or suggestion of "defining a functional model in a high level language for simulating the architectural behavior of the ASP, wherein the functional model CPU and a set of peripherals are defined." In the method of development disclosed by Bona, prior to actual fabrication of the circuit, a simulated circuit is tested on a workstation. However, Bona does not disclose, teach, or suggest that the simulation is a functional model defined in a high level language. Second, claim 1 also recites "generating for each peripheral an interface functions file which defines the communication attributes of the peripheral with the processor and the functional attributes of the peripheral in a manner independent of any particular data structure, and a test functions file which defines the communication attributes of the processor with the peripheral in a manner independent of any particular data structure." Clearly, Bona fails to disclose this limitation as the peripherals in Bona are simulated using discrete hardware components on the test platform such as memory 111 and 112 which are used to emulate the RAM and ROM memory of the ASIC. Third, Bona clearly does not disclose "simulating in the high level language as part of the functional model an application executable by the CPU and operations of the set of peripherals for a predetermined simulation phase, the application executable by the CPU including the test functions file and the operations of the set of peripherals including the interface functions file," as recited in claim 1. As discussed above, Bona discloses writing the application software and validating it on the test board in step T of Fig. 4A. Thus, since Bona discloses actually writing the application software, Bona clearly does not disclose simulating the software in a high level language as part of a functional model of the

circuit. Lastly, Bona does not disclose "converting the modelling file in the high level language to a simulation language for simulating the ASP at circuit level" and "simulating the ASP at circuit level using the simulation language for a subsequent simulation phase" as recited in claim 1. Indeed, since the method of development of an ASIC in Bona does not even disclose a functional model in a high level language, Bona clearly cannot possibly disclose, teach, or suggest generating a modelling file containing output state information of the circuit peripherals and then using this modelling file to create a simulation of the ASP at the circuit level as recited in claim 1. In fact, as shown in Fig. 4A, the only simulation of the circuit in Bona is already at the circuit level. Thus, Bona clearly does not disclose converting a modelling file in the high level language to a simulation language. Since Bona does not disclose any of the above-noted limitations recited in claim 1, claim 1 patentably distinguishes over Bona. According, it is respectfully requested that the rejection of claim 1 under 35 U.S.C. §102(a) be withdrawn.

Claims 2-5 depend from claim 1 and are patentable for at least the same reasons as discussed above in connection with claim 1. Accordingly, it is respectfully requested that the rejection of claims 2-5 under 35 U.S.C. §102(a) be withdrawn.

Claim 6 is directed to a computer system for simulating an ASP. The computer system of claim 6 comprises "first processor means including execution means for simulating a functional model in a high level language and output means for outputting the state of the functional model at the end of a predetermined simulation phase." As discussed above Bona does not disclose a functional model in a high level language. Thus, it would be impossible for Bona to disclose simulating this functional model and outputting the state of the functional model. The computer system of claim 6 further comprises "means for converting the functional model, including its state at the end of the predetermined simulation phase into a simulation for simulating the ASP at circuit level." Again, since Bona does not disclose a functional model, it is impossible for Bona to disclose or suggest converting the functional model into a simulation language. Since Bona fails to disclose or suggest these limitations of claim 6, claim 6 patentably distinguishes over Bona. Accordingly, it is respectfully requested that the rejection of claim 6 under 35 U.S.C. §102(a) be withdrawn.

Claim 7 is directed to a modelling file which comprises "a first code portion holding a test functions file defining the communication attributes of a processor with a peripheral of an ASP to be simulated and including the state of the test functions file after a predetermined

simulation phase and a second code portion holding interface functions file which defines the communication attributes of the peripheral with the processor and the functional attributes of the peripheral and including the state of the interface functions file after a predetermined simulation." Bona does not disclose or suggest a modelling file as recited in claim 7. As discussed above, Bona only discloses modelling the ASIC at the circuit level, and thus contains no disclosure or suggestion of a modelling file as required by claim 7. Thus, claim 7 patentably distinguishes over Bona. Accordingly, it is respectfully requested that the rejection of claim 7 under 35 U.S.C. §102(a) be withdrawn.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to deposit account No. 23/2825.

Respectfully submitted,

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